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Monday, October 13. 2008

The architecture of the SPARC Enterprise T5440

Denis Sheahan wrote two insightful articles to the architecture of the T5440. The first one is about the architecture of the system in general. The system is really an elegant design. By the the way: The similarities to the X4600 chassis are not an accident

The second one is about a chip, that made this system possible at all - the Zambezi ASIC:Coming out of each UltraSPARC T2 Plus processor are 4 independent coherence planes. The T2 plus has 8 banks of L2 cache and each plane is responsible for the traffic from two of these banks. The plane is identified by two bits (12 and 13) of the Physical address. There are 4 Zambezi hubs in the system, each handling a single coherence plane. Each Zambezi is connected to each of the four T2 Plus processors over four separate point-to-point serial coherence links Because planes are independent there are no connections between the Zambezi chips.

Posted by Joerg Moellenkamp in English, Oracle at 20:44

Der Zambesi link verweist auf ne schöne Seite, ist aber trotzdem falsch
Anonymous on Oct 13 2008, 22:46

Korrigiert
Anonymous on Oct 14 2008, 06:04